# On-chip to off-chip clocking interfaces from academia to industry : A integrated approach to clock generation and distribution

**Niraj Bindal – Intel India**
Contact Author: Niraj.bindal@intel.com

1. Tutorial title and short summary (in about 200 words).

Understanding the context of clocking problem is key to anticipating future clocking solutions for any researcher in academia. This tutorial will bridge several gaps in clocking tutorials commonly presented at conferences by contrasting the academic and industrial approaches to clocking solutions without favoring any particular CAD tool or solution. First, it covers the interrelationship of clock distribution vs. clock generation strategy for a design project. Second, academia needs to understand non-algorithmic trade-offs in choice of industrial applications of clock and circuit solutions. Third, on-chip clocking vs. off-chip clocking on mother boards have very different metrics of optimization, which need to be adequately considered while designing clock circuits for various input-output architectures, or extending on-chip algorithms to off-chip solutions.

The tutorial covers (a) industrial clocking problem statement, (b) CAD algorithms for clock distribution, (c) industrial clock distribution case-studies from Intel and IBM emphasizing salient characteristics of desired off-chip and on-chip solutions each for 1 hour (total of 3 hours) in the first module. The second module covers clock generation basics for (d) Ist order systems (DLLs) with components like delay line, charge pump, phase detector,, (e) 3rd order analog systems(PLL) with components like VCO (voltage controlled oscillator), loop filter, and (f) fully digital approaches, each for 45 mins, followed by a (g) concluding look at full clocking system on a mother-board with dive into every chip sub-system for 30 mins. Each module will include an engaging 10 min quiz to help audience keep pace.

2. Name, affiliation and contact details of the co-ordinating presenter and all other co-presenters.

Niraj Bindal – Intel Technologies India Pvt Ltd
Microprocessor Design Group
Bangalore Design Center
Mobile Phone : 984 547 8915
Email : niraj.bindal@intel.com

3. The targeted audience and prerequisites (in about 50 words).

Masters in engineering students or higher, interested in understanding a hierarchy of clocking problem statements with practical considerations.

Industry clock designers looking for update on latest published research in clock distribution, generation and clocking for synchronous IO circuits.

Basic circuit design knowledge required. Basic knowledge of algorithms, complexity, and data structures will be helpful. Should be able to understand VLSI manufacturing process, and in case of PLL's understand fundamentals of control theory, Laplace transforms, Fourier series and bode-plots.

4. Keywords from those listed in the topics above, or otherwise.

Clock distribution, H-tree, MMM (method of means and medians), GMA (geometric mean algorithm), partitioning, ZSK (zero skew algorithm), DME (deferred merged and embedding algorithm) and its variations, recombinant trees, buffered trees, inductive trees, point-to-point distribution, termination impedance, obstacle aware routing, clock skew, clock jitter

Clock generation, PLL (phase locked loop), DLL (delay line loop), ADPLL (All digital phase lock loop), drift jitter, thermal noise, flicker noise, LC-PLL (inductive capacitive phase lock loop)

5. Detailed tutorial program, with a list of topics covered, a short description of each topic and the approximate time devoted to each topic (in about 2000 words). (Full day tutorials will be six hours and half day tutorials will be three hours ).

The tutorial covers

(a) industrial clocking problem statement, (55 minutes including 10 min quiz, 5 min break)

1. Understanding functional failure (hold-time violation) is different than a speed path failure (max-time violation)
2. Clock distribution problem statement includes differentiating between clock skew and clock jitter, sources of clock skew, sources of clock jitter in an industrial design.
3. Industrial for clock distribution design cycle requires adapting to flexible specifications and need for incremental design.
4. Formal clock distribution problem statement & 5 minute quiz
5. Clock generation problem statement includes frequency multiplication and hiding clock distribution delay.
6. Industrial clock generation problem relates to testability of clocking, and using clocking to test the rest of the chip. Describe jitter prediction and measurement techniques need to be supported by the cost-benefit trade-off goals of the design.
7. Formal clock generation problem statement & 5 min quiz

(b) CAD algorithms for clock distribution, (55 minutes including 10 min quiz, 5 min break)

1. Review of basic algorithms : MMM, ZSK, GMA, DME and most variations of DME
2. Review industrial constraints like varying loads, obstacle awareness, multiple metal layers, delay awareness, cross-coupling reduction, incremental design cycle
3. Comparative study of various algorithms and differing applications for each algorithm.

(c) Industrial clock distribution case-studies emphasizing salient characteristics of desired off-chip and on-chip solutions (55 minutes including 10 min quiz, 5 min break)

1. Case study of custom designed buffered tree & de-skew mechanisms by Intel Corporation
2. Case study of custom designed interconnect based trees by IBM
3. Case study of custom designed recombinant trees by DEC Alpha
4. Case study of fully synthesized clock distribution tree
5. Case study of off-chip clock distribution design

(d) Ist order clock generation circuit – Delay line loop (45 minutes including 10 min quiz),

1. Basic architecture,
2. Phase detector circuit, and Laplace model
3. Delay line circuit, and Laplace model
4. Charge pump circuit and Laplace model
5. Full loop operation and Laplace model, with basic pole-zero understanding
6. Circuit design and modeling challenges, with success metrics

(e) 3rd order analog clock generation circuit - Phase lock loop (55 minutes including 10 min quiz),

1. Basic architecture,
2. LC PLL, crystal based PLL,
3. VCO – voltage controlled oscillator circuit and Laplace model
4. Loop filter – circuit and Laplace model
5. Full-loop model stability analysis, with circuit implications
6. Sources of noise and jitter injection, and amplification
7. PLL, DLL architecture for source synchronous IO

(f) fully digital approaches, ADPLL (All digital PLL) (35 minutes including 10 min quiz, 5 min break)

1. Desire for fully digital approach – problems with analog design
2. Testability and measuring jitter
3. Phase synthesis and testing digital circuits by clock wave manipulation

(g) concluding look at full clocking system on a mother-board with dive into every chip sub-system (30 minutes including 5 min quiz)

6. Indicate if the proposal is for full day tutorial or half day tutorial.
YES. The proposal is for a 6-hour, full day tutorial.

7. Technical bibliography (with emphasis on the authors' works and other related works being covered).

(a) Course material from full semester special topics 40 hr long course on “Clock generation and distribution” OSU-679C taught by the author(Niraj Bindal) as invited guest professor at Oregon State University, Fall 2000. The material covered roughly 3-4 published papers every hour. The course was aimed at senior masters and aspiring PhD students at the department of Electrical and Computer Engineering.

(b) Invited session note talk: Challenges in Clock Distribution Networks, ACM/SIGDA International Symposium on Physical Design April 12-14, 1999, Monterey, California. Niraj Bindal, Strategic CAD Labs, Intel Corporation, Hillsboro, Oregon

(c) Algorithms for VLSI Physical Design Automation, second edition, Naveed Sherwani, Chapter-9: Specialized routing, authored by Niraj Bindal.

(d) A Scalable Sub-10ps Skew Global Clock Distribution for 90 nm Multi-GHz IA Microprocessor, Niraj Bindal, Timothy Kelly, Nicholas Velastegui, Keng L Wong, Intel Corporation, ISSCC – International Solid State Circuits Conference 2003

8. List of tutorial material to be provided to the attendees.

Only quiz material is planned.

Foil set could be made available if required by the conference tutorial chair.

9. Short biographical sketch of each presenter indicating previous experience in delivering lectures and tutorials, and expertise on the tutorial topic. (About 200 words for each presenter).

Niraj Bindal has been at Intel corp for over 18 years in various positions as VLSI design engineer and lead for clock circuits and systems, thermal circuits, circuit robustness analysis methods, SRAM and Flash memory cell designs. He has designed portions of 7 microprocessor chips, 2 SRAM chips and 1 Flash memory chip, including a 3 year rotation in research at Intel's Strategic CAD Labs. He has experience in design lead of all circuit subsystems of phase-lock loops, synchronous IO circuits, band-gap circuits and methodologies for clock distribution and synthesized logic blocks. He also specializes in statistical theory for robust manufacturability of analog and digital circuits due to within-die variations in sub-micron technologies including latest 45 nm.

Niraj has special interest in research, and teaching. He has been an invited guest professor at Oregon State University and OCATE while working at Intel – Hillsboro Oregon before relocating to Intel India. He also has a passion for studying methods of teaching, and as a hobby teaches high school Maths and physics in his spare time. Niraj has been sought after by publishers several times to compile a book on clocking. He has authored chapters in text books on physical design and published leading edge clock design papers representing Intel corporation.